REMARKS

Claims 1 and 53 have been amended, and corresponding amendments have been made to withdrawn dependent claims 4, 7, 15, 20-21, 37-38, 47, 56 and 58. Claims 17, 36, 39, 43-46, and 50 have been canceled. Claims 59-66 have been added. Claims 1, 3-12, 14-16, 18, 20-21, 28-29, 31-34, 37-38, 40-42, 47-49 and 53-66 are pending.

Claims 1 and 53 stand rejected as being unpatentable over Asnaashari (U.S. Patent No. 6,076,137) and Ellis (U.S. Patent No. 6,029,226). This rejection is respectfully traversed.

Claim 1 recites, *inter alia,* "An integrated input/output controller ... for transceiving data as a plurality of data blocks between one host and a disk array, comprising a host interface subsystem ... including a command decode controller;... a RAID mapping controller ... for mapping logical block addresses of the data flow type host commands into disk block addresses of a plurality of disks of a RAID disk array; and a disk interface subsystem ... for transceiving said data blocks with the plurality of disks using the disk block addresses generated by the mapping controller; wherein, for each data flow type host command, said command decode controller communicates an associated logical block address to the mapping controller, said mapping controller converts the associated logical block address to an associated disk block address, and said disk interface subsystem accesses the plurality of disks using said associated disk block address."

Asnaashari is directed to a controller for a flash memory system, i.e., a solid-state memory, not a RAID disk array. Flash memory systems have peculiar characteristics. For example, in a flash memory, which is organized into blocks, the contents of a

previously written block cannot be rewritten unless the block is first erased in a lengthy erase procedure. Further, each block of a flash memory can only be erased and rewritten a finite number of times before the block malfunctions. Asnaashari discloses a controller for a flash memory which works around these limitations of the flash memory technology. In particular, Asnaashari's controller performs a mapping between logical addresses asserted by a user of the flash memory to physical addresses used by the controller to improve performance and equalize wear across the blocks of the flash memory. See column 3, line 26 – column 4, line 40.

Claim 1, as amended, specifically recites a RAID mapping controller for mapping logical block addresses asserted by at least one host into disk block addresses of a plurality of disks in a RAID disk array, and further recites a disk interface system for transceiving data blocks between the host and the RAID disk array. Asnaashari fails to teach or suggest these features, as the mapping described in Asnaashari is directed to managing the particular characteristics of a flash memory system, which are vastly different from those associated with a RAID disk array. For example, RAID disk arrays utilize redundancy information in the form of mirroring and/or parity, and may stripe data across multiple disk drives. These features are not found in flash memory systems. Flash memory is not analogous to RAID disk arrays. Accordingly, it is not surprising that the above noted features of the present invention are not taught or suggested by Asnaashari.

Ellis discloses a method for writing data to a disk drive. More specifically, Ellis discloses that a first write command to a storage device can be buffered. When a second write command is received, under certain circumstances both write commands are processed at as a single write command to the storage device. Ellis, however, also fails to teach or suggest the above recited features recited in claim 1, specifically an integrated

input/output controller for a RAID disk array. Indeed, Ellis does not even disclose an **integrated** command decoder (for which it was cited) – rather, only the storage device in Ellis is integrated.

For the foregoing reason, claim 1 is submitted to be allowable over the prior art of record. Dependent claim 53 , and the dependent claims which have been withdrawn from consideration, are also submitted to be allowable for at least the same reasons as claim 1.

New claims 59-66 recite limitations directed to certain operational characteristics of disk arrays. These features are not taught or suggested by the prior art of record. For example, claim 65 recites that the disk interface includes a SCSI initiator. This feature is also not taught or suggested by the prior art of record. Claim 66 recites the use of plural logical volumes and further recites that the controller independently processes commands directed to he logical volumes. This feature is not taught or suggested by the prior art of record. Accordingly claims 59-66 are believed to be allowable for these additional reasons.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By _____

Stephen A. Soffen
Registration No.: 31,063
Christopher S. Chow
Registration No.: 46,493
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant